ABSTRACT OF THE DISCLOSURE

A multiplication circuit and a phase synchronization circuit as components of a digital PLL circuit adjust an oscillation frequency and a phase, respectively, of a multiplied clock by adjusting a count value of a digital counter. A CPU sets a count value for oscillating an oscillation circuit of the multiplication circuit at a frequency which is the same as that of a reference clock or is a multiple of the frequency of the reference clock in a digital counter of the multiplication circuit in accordance with a program set by the user of the information processing apparatus, and sets a count value for synchronizing the phase of an output clock with the phase of the reference clock in a digital counter of the phase synchronization circuit.